

N68-VS3 UCC

G/A1.01

ATX Power

+5VSB +12V
+3.3V -5V
+5V -12V

PAGE : 3

System Regulator

INPUT OUTPUT
+5VSB +3VSB
+3VDUAL +1.2DUAL
+3V +2.5V
VCCM VTT_DDR

PAGE : 4

CPU DC/DC

RT8857

INPUT OUTPUT
+12V +1.85V~1.1V

PAGE : 5

MCP68 DC/DC

INPUT OUTPUT
VCCM +1.2V

VCCM DC/DC

RT8105PS

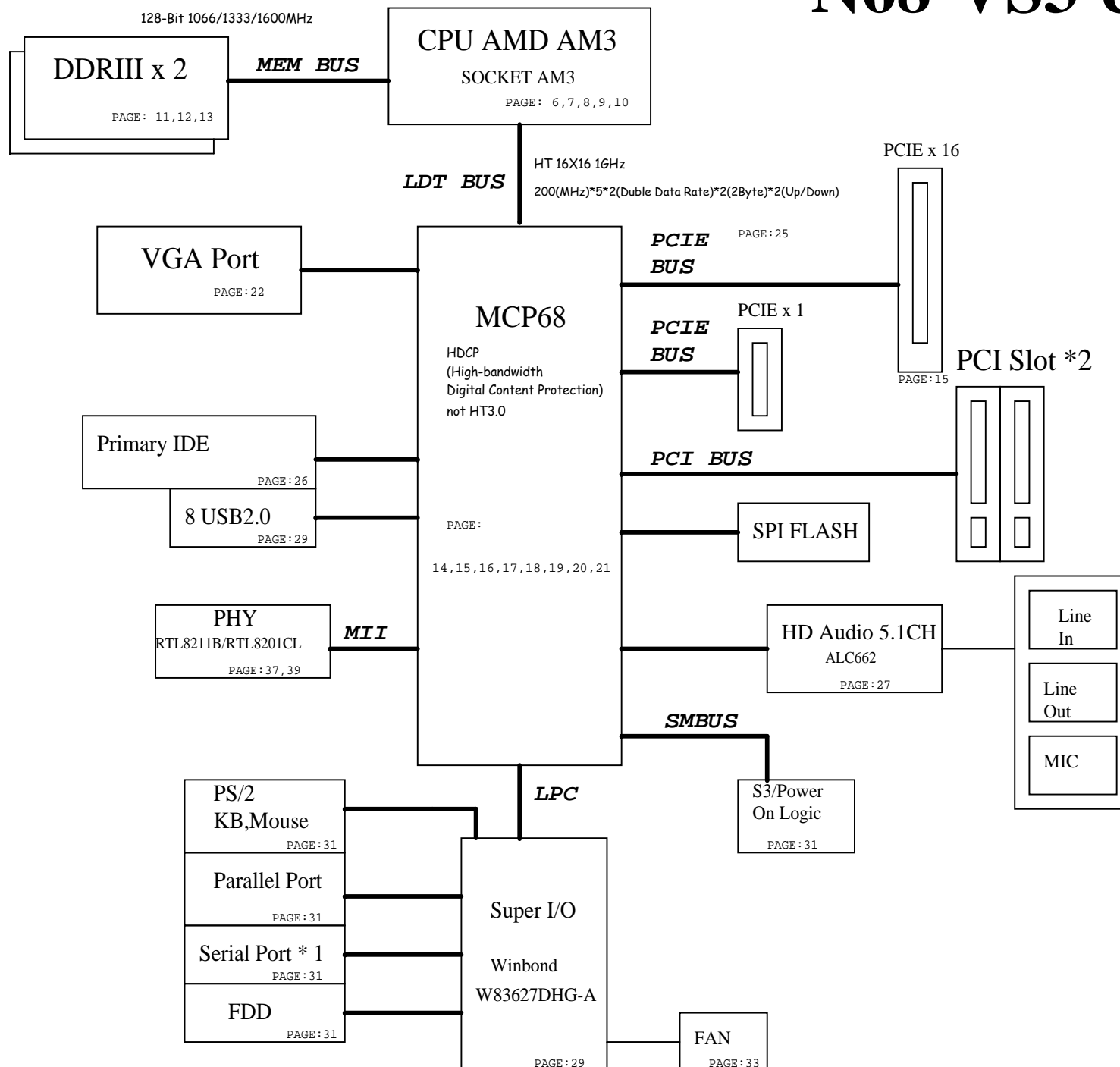
INPUT OUTPUT
+5V +1.8V

PCB LAYER

L1 : Component (S1)
L2 : VCC
L3 : GND
L4 : Component (S4)

<Core Design>

ASRock ™ Title : BLOCK		
ASROCK Inc.		Engineer: Mingus_Wu
Size A4	Project Name N68-VS3 UCC	Rev 1.01
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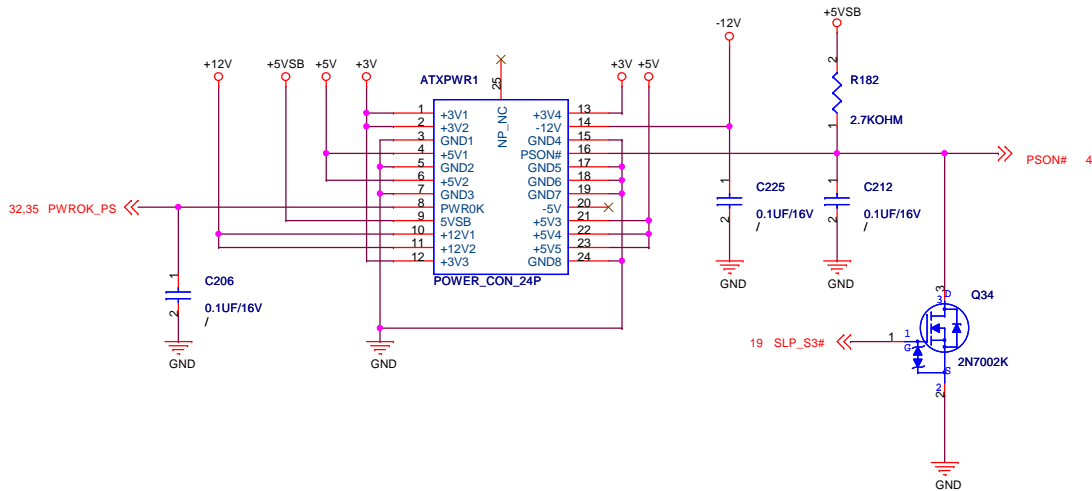


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1	BLOCK	ARCHITECTURE BLOCK DIAGRAM
2	HISTORY	HISTORY OF MAIN BOARD VERSION
3	ATXPWR	ATX Power Conn(+3.3V, +5V, +12V)
4	SYSTEM PWR	SYSTEM Linear Power
5	CPUPWR	DC/DC FOR CPU
6	K8_M2_A	AMD Socket M2 HDT
7	K8_M2_B	AMD Socket M2 DDRII
8	K8_M2_C	AMD Socket M2 MISC (CPU CTRL. & DEBUG)
9	K8_M2_D	AMD Socket M2 POWER & GND
10	K8_M2_E	AMD Socket M2 POWER & GND
11	DDRII SLOT 1	DDRII SLOT 1
12	DDRII SLOT 2	DDRII SLOT 2
13	DDR2 TERMINATION	DDR2 TERMINATION
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15	MCP61-2	MCP61 PCIE X16
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17	MCP61-4	MCP61 PCI/LPC
18	MCP61-5	MCP61 SATA/IDE
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20	MCP61-7	MCP61 PWR/GND
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22	VGA	ON_BOARD VGA
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24	PCI SLOT X2	PCI1/2 SLOT
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26	SPI	SPI
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28	AUDIO CON.	ALC662 6CH. AUDIO CONNECTOR
29	SIO W83627DHG-A	SIO W83627DHG-A (FAC)
30	USB PORT	USB PORT 2&3, 4&5, 6&7
31	IO CONNECTOR	PS2KB/MS, FDD, COM1, PARALLEL
32	PWR SEQUENCE, S3	NVIDIA PWR SEQUENCE, S3
33	PANEL	I/O PANEL
34	SCREW & EUP	SCREW, BYPASS CAP, EUP.
35	+1.2V Power	VCCM to +1.5V, +1.5V to +1.2V
36	VCCM SWITCH	SINGLE PHASE (RT8105PS)
37	LAN PHY	10/100 LAN PHY_RTL8201CL
38	OTHER CAP.	OTHER CAP.

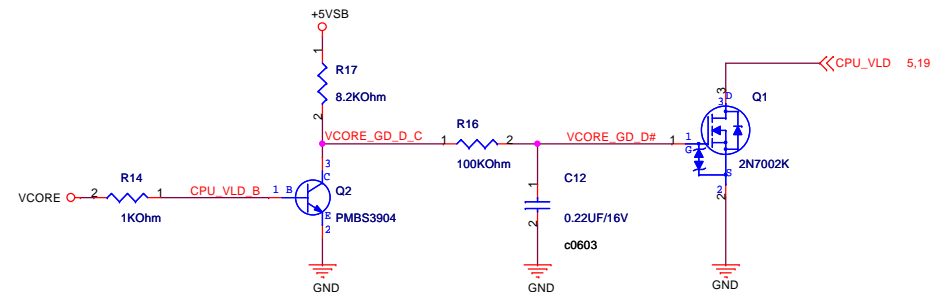
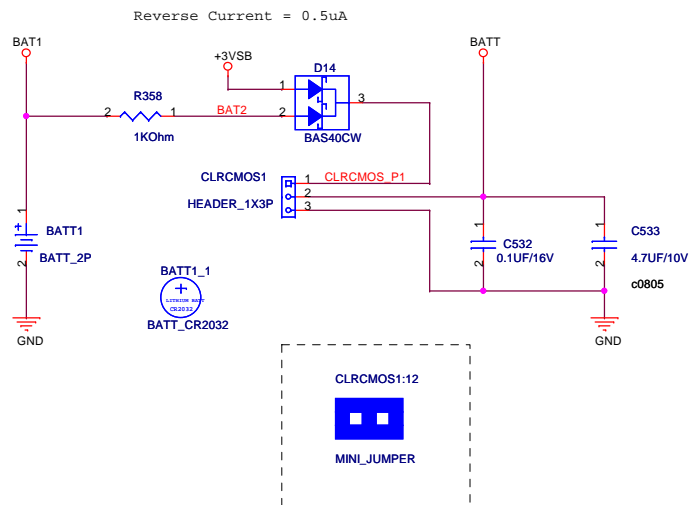
Revision History

Date	Version	Change Note

ATX POWER

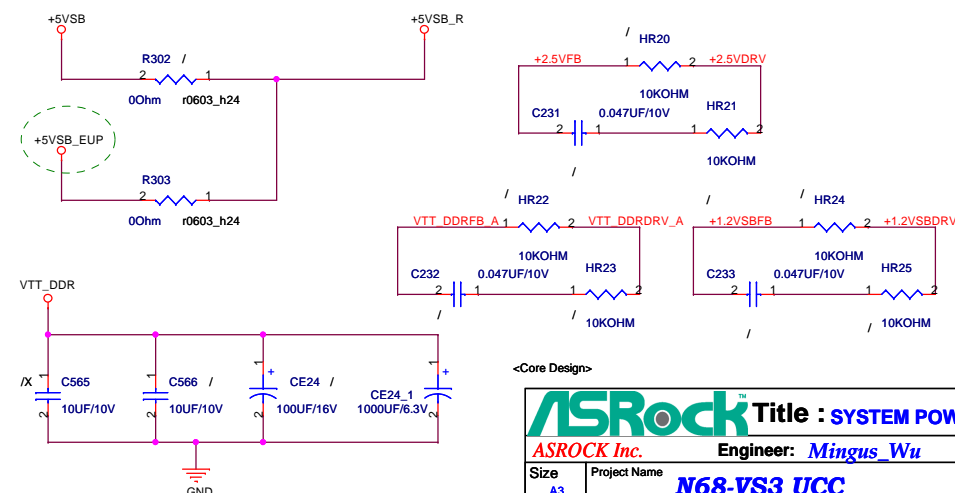
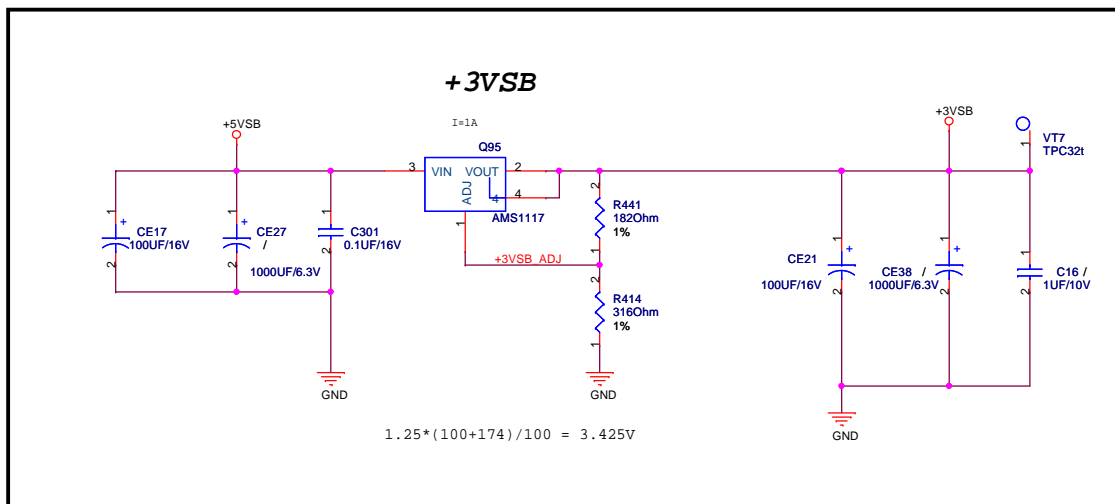
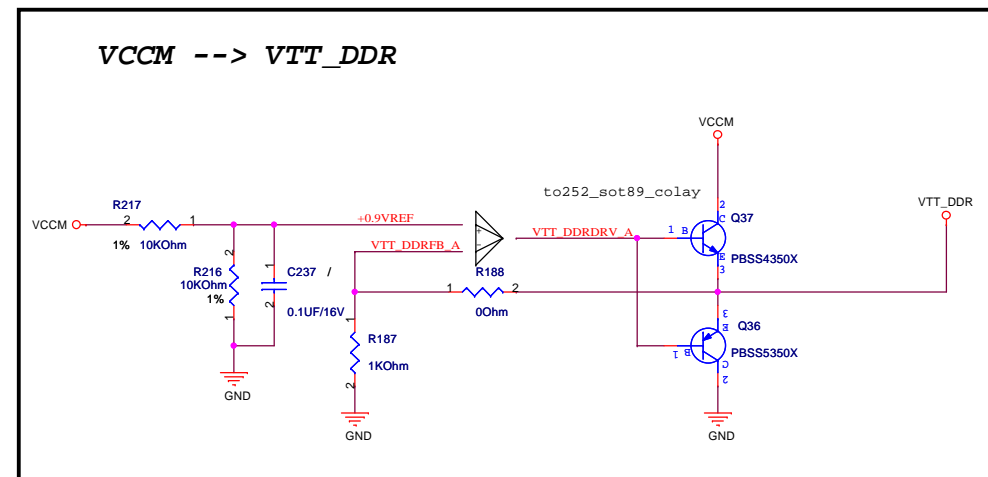
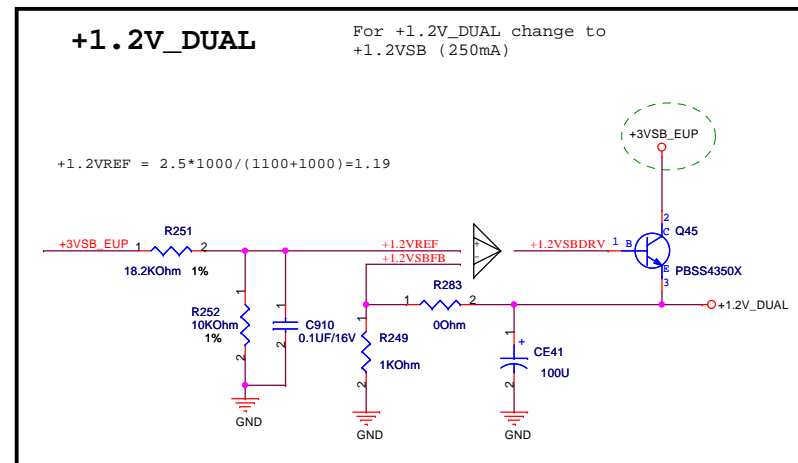
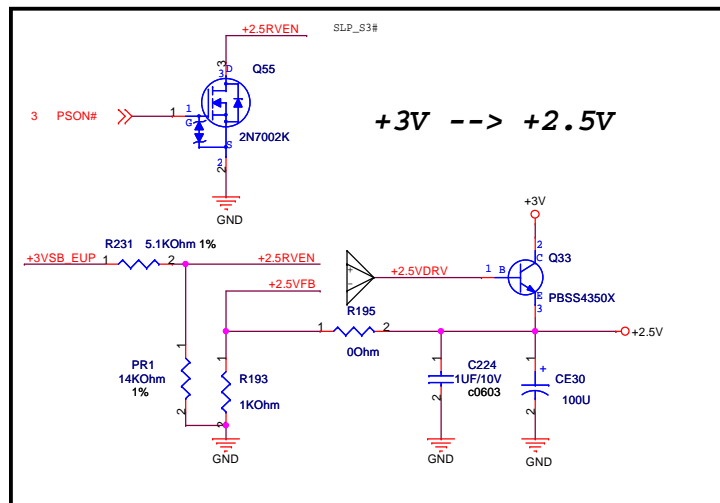
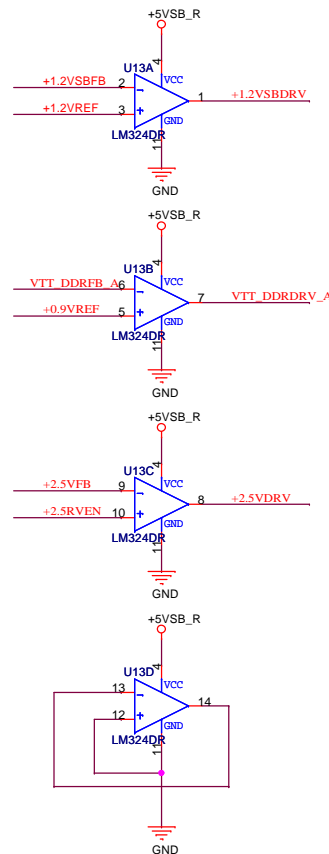
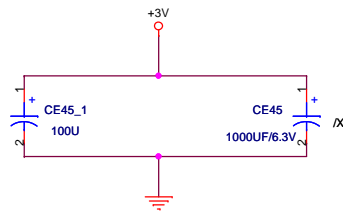


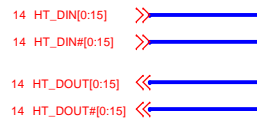
BATT



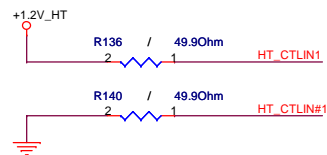
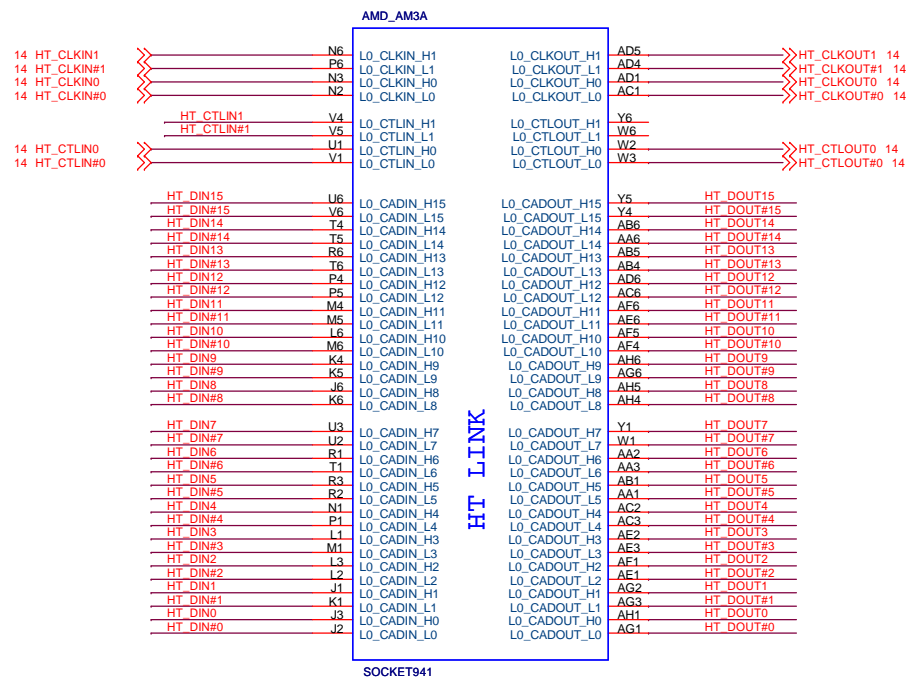
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ASRock		Title : ATX POWER	
ASROCK Inc.		Engineer: Mingus_Wu	
Size A3	Project Name N68-VS3 UCC	Rev 1.01	
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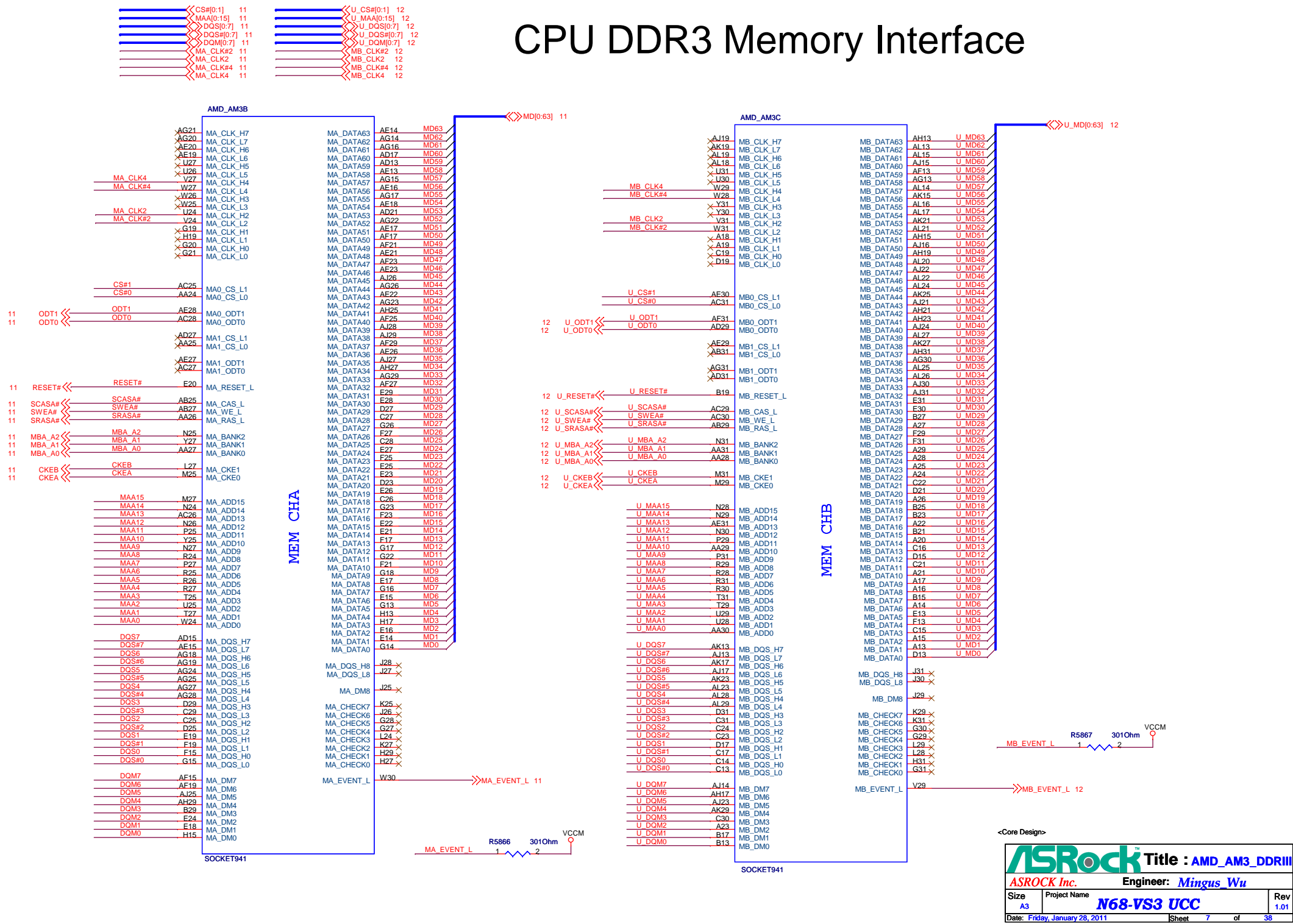


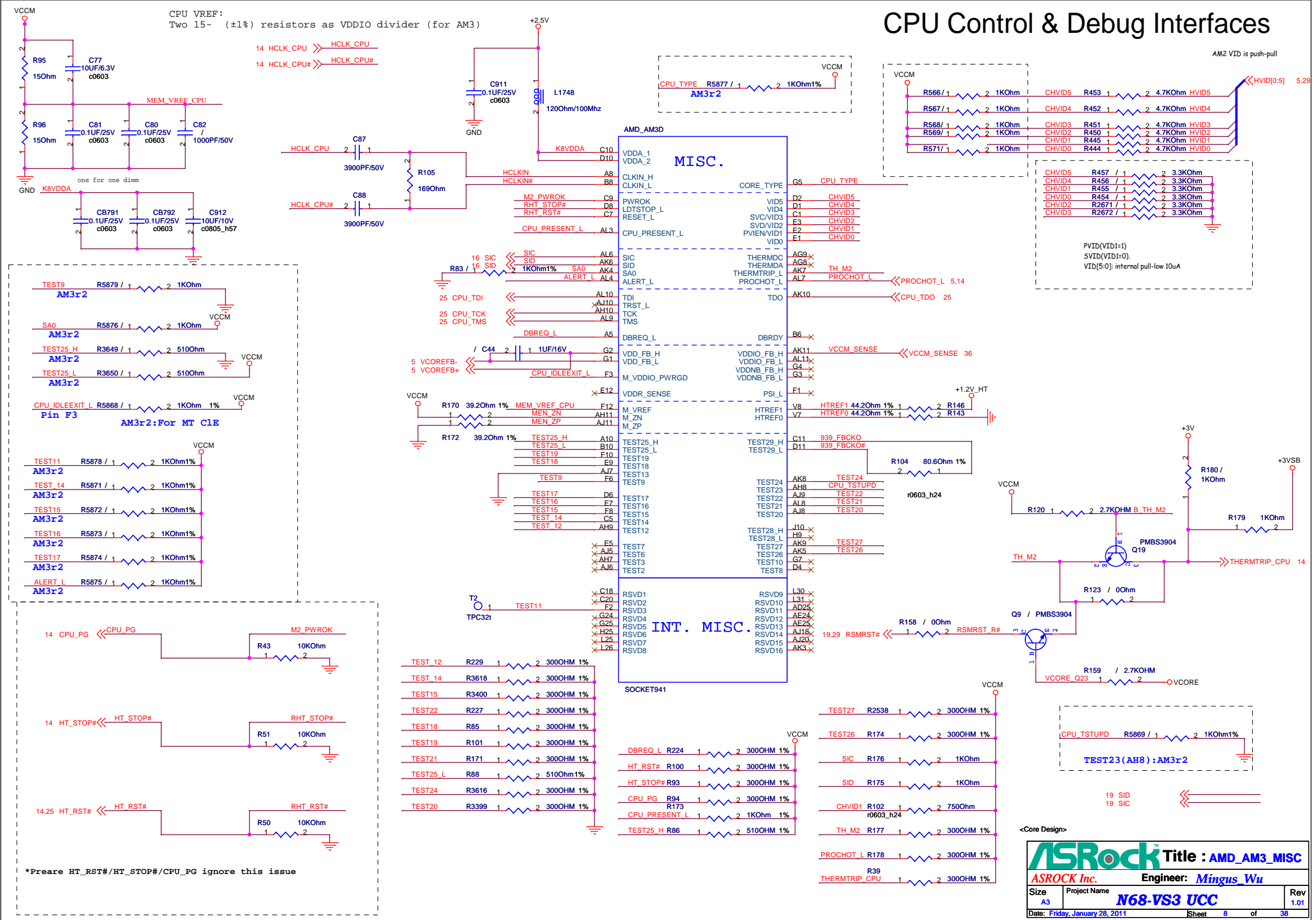
CPU HyperTransport Interface



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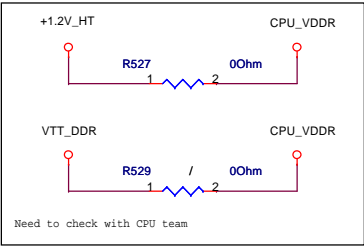
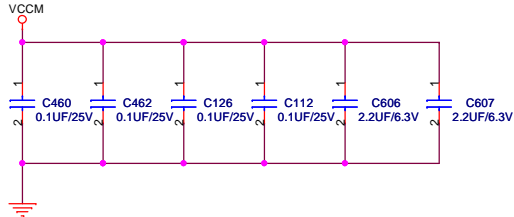
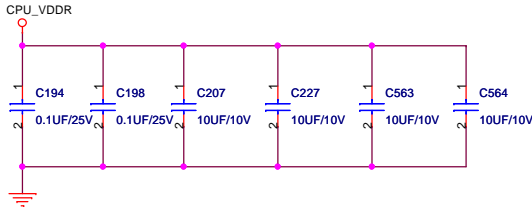
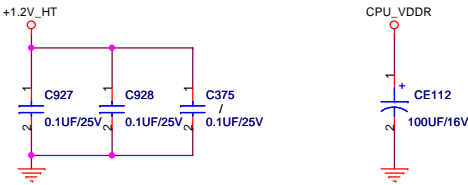
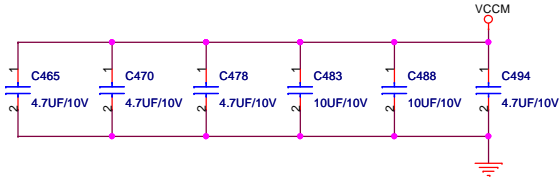
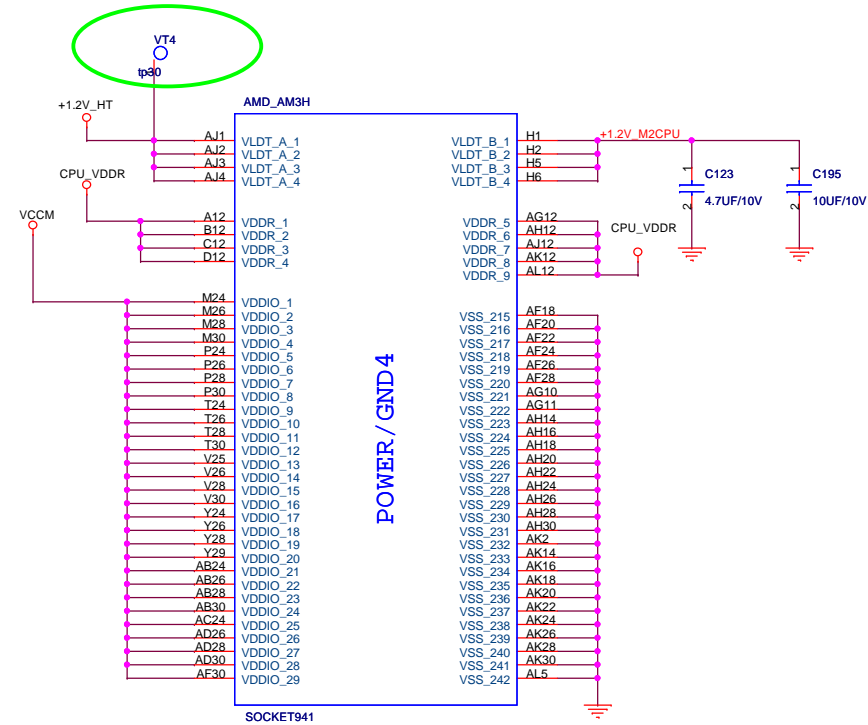
CPU DDR3 Memory Interface






Hammer VID Codes

VID4	VID3	VID2	VID1	VID0	VCORE (V)
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	OFF



<Core Design>

**Title : AM3_GROUND**

ASROCK Inc. Engineer: **Mingus Wu**

Size **A3** Project Name **N68-VS3 UCC** Rev **1.01**

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DDR SLOT1

DDR3_A1A A0

DDR3_A

MD[0:63] 7

MAA0 188
MAA1 181
MAA2 61
MAA3 180
MAA4 59
MAA5 58
MAA6 178
MAA7 56
MAA8 177
MAA9 175
MAA10 70
MAA11 55
MAA12 174
MAA13 196
MAA14 172
MAA15 171

MA_CLK2 63
MA_CLK#2 64
MA_CLK4 184
MA_CLK#4 185

CS#1 76
CS#0 193

7 ODT1 77
7 ODT0 195

7 SWEA# 73
7 SRASA# 192
7 SCASA# 74

7 MBA_A2 52
7 MBA_A1 190
7 MBA_A0 71

7 CKEB 169
7 CKEA 50

119
237
117

DQS7 112
DQS#7 111
DQS6 103
DQS#6 102
DQS5 94
DQS#5 93
DQS4 85
DQS#4 84
DQS3 33
DQS#3 33
DQS2 25
DQS#2 24
DQS1 16
DQS#1 15
DQS0 7
DQS#0 6

DQM7 230
DQM6 221
DQM5 212
DQM4 203
DQM3 152
DQM2 143
DQM1 134
DQM0 125

12,19,34 SMBCLK 118
12,19,34 SMBDATA 238

162
231
222
213
204
153
144
135
126

DDR3_DIMM_240P

A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12
A13
A14
A15
CK1/NU
CK1/NU#
CK0
CK0#
S1#
S0#
WE#
RAS#
CAS#
BA2
BA1
BA0
CKE1
CKE0
SA2
SA1
SA0
DQS7
DQS7#
DQS6
DQS6#
DQS5
DQS5#
DQS4
DQS4#
DQS3
DQS3#
DQS2
DQS2#
DQS1
DQS1#
DQS0
DQS0#
DM7/DQS16
DM6/DQS15
DM5/DQS14
DM4/DQS13
DM3/DQS12
DM2/DQS11
DM1/DQS10
DM0/DQS9
SCL
SDA
DQS17#
DQS16#
DQS15#
DQS14#
DQS13#
DQS12#
DQS11#
DQS10#
NC/DQS9#

CB7 165
CB6 164
CB5 158
CB4 46
CB3 45
CB2 40
CB1 39
CB0

DQS8 43
DQS8# 42

DM8/DQS17
VTT2
VTT1

RESET#

RSVD
NC/PAR_IN
NC/ERR_OUT
NC/TEST4
FREE1
FREE2
FREE3
FREE4
P_NC1
P_NC2
P_NC3

79
68
53
167
198
187
49
48
241
242
243

MA_EVENT_L 7

165
164
159
158
46
45
40
39

VTT_DDR

RESET# 7

MA_EVENT_L 7



CS# [0:1] 7
MAA [0:15] 7
DQS [0:7] 7
DQS# [0:7] 7
DQM [0:7] 7
MA_CLK#2 7
MA_CLK2 7
MA_CLK#4 7
MA_CLK4 7

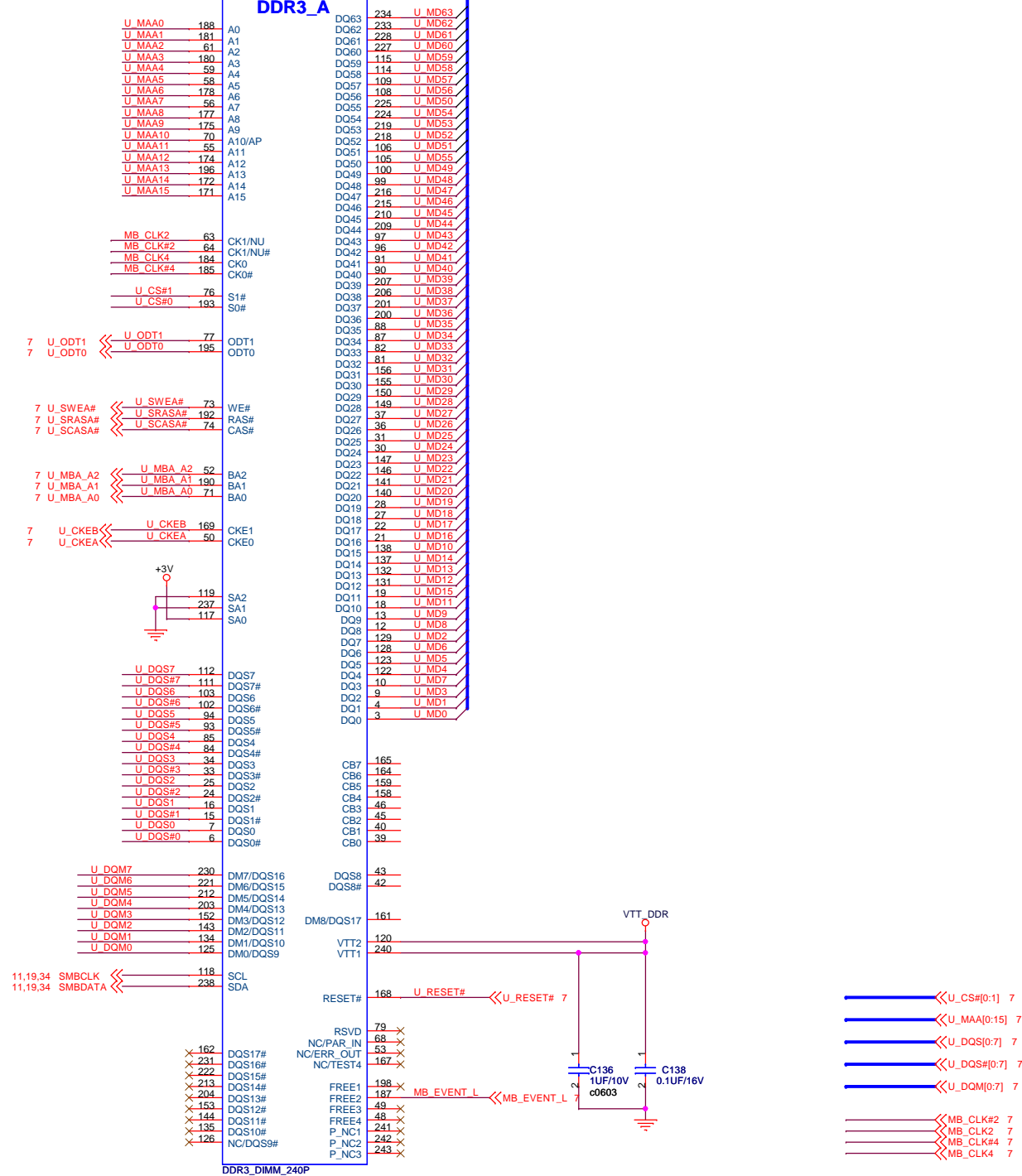
<Core Design>

ASRock Title : DDR3_DIMM1	
ASRock Inc. Engineer: <u>Mingus_Wu</u>	
Size A3	Project Name N68-VS3 UCC
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DDR SLOT2

DDR3_B1AA2

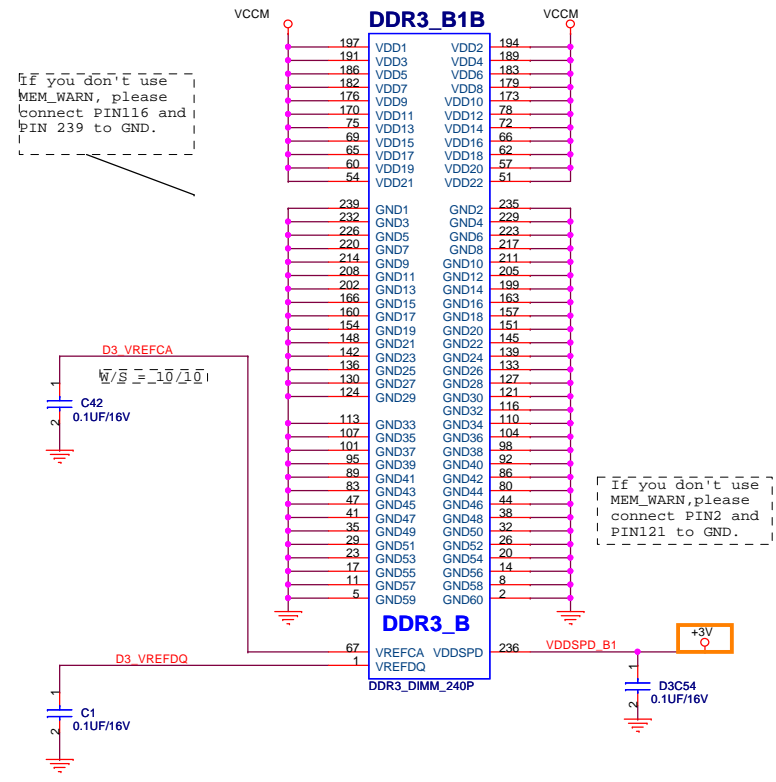
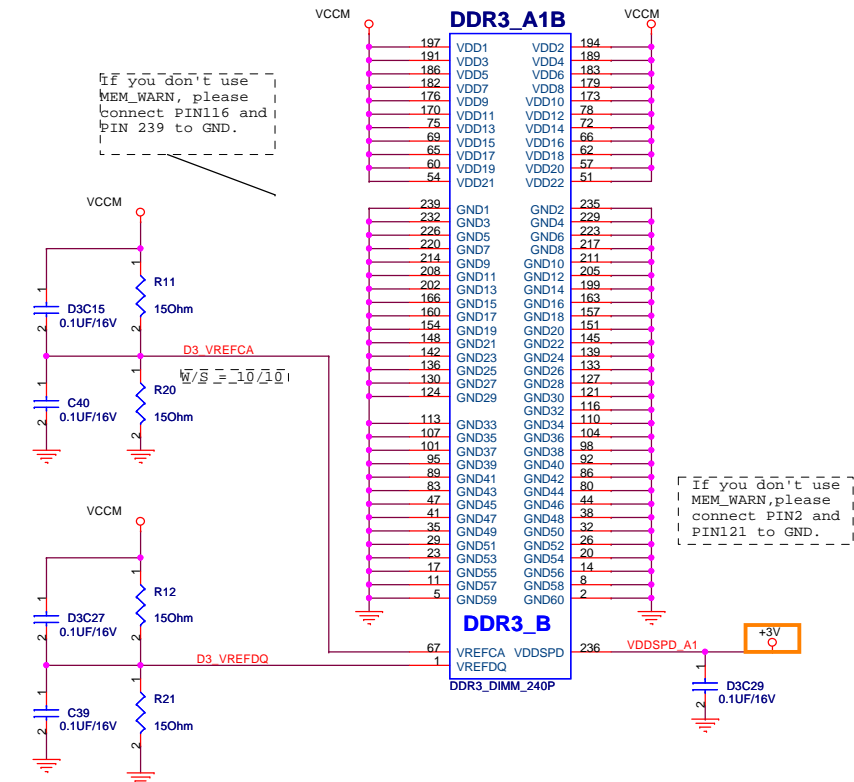
DDR3_A



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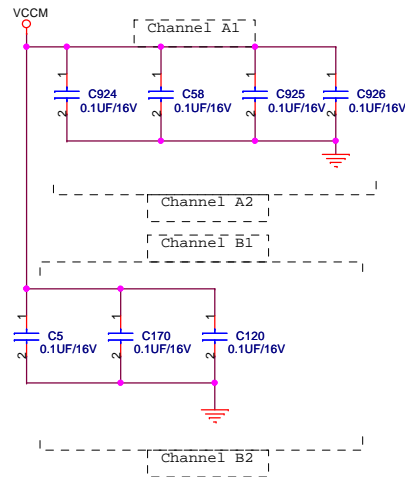
ASRock™ Title : DDRIII_DIMM2

ASROCK Inc.		Engineer: <u>Mingus_Wu</u>	
Size A3	Project Name N68-VS3 UCC	Rev 1.01	
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If you don't use MEM_WARN, please connect PIN116 and PIN 239 to GND.

If you don't use MEM_WARN, please connect PIN116 and PIN 239 to GND.

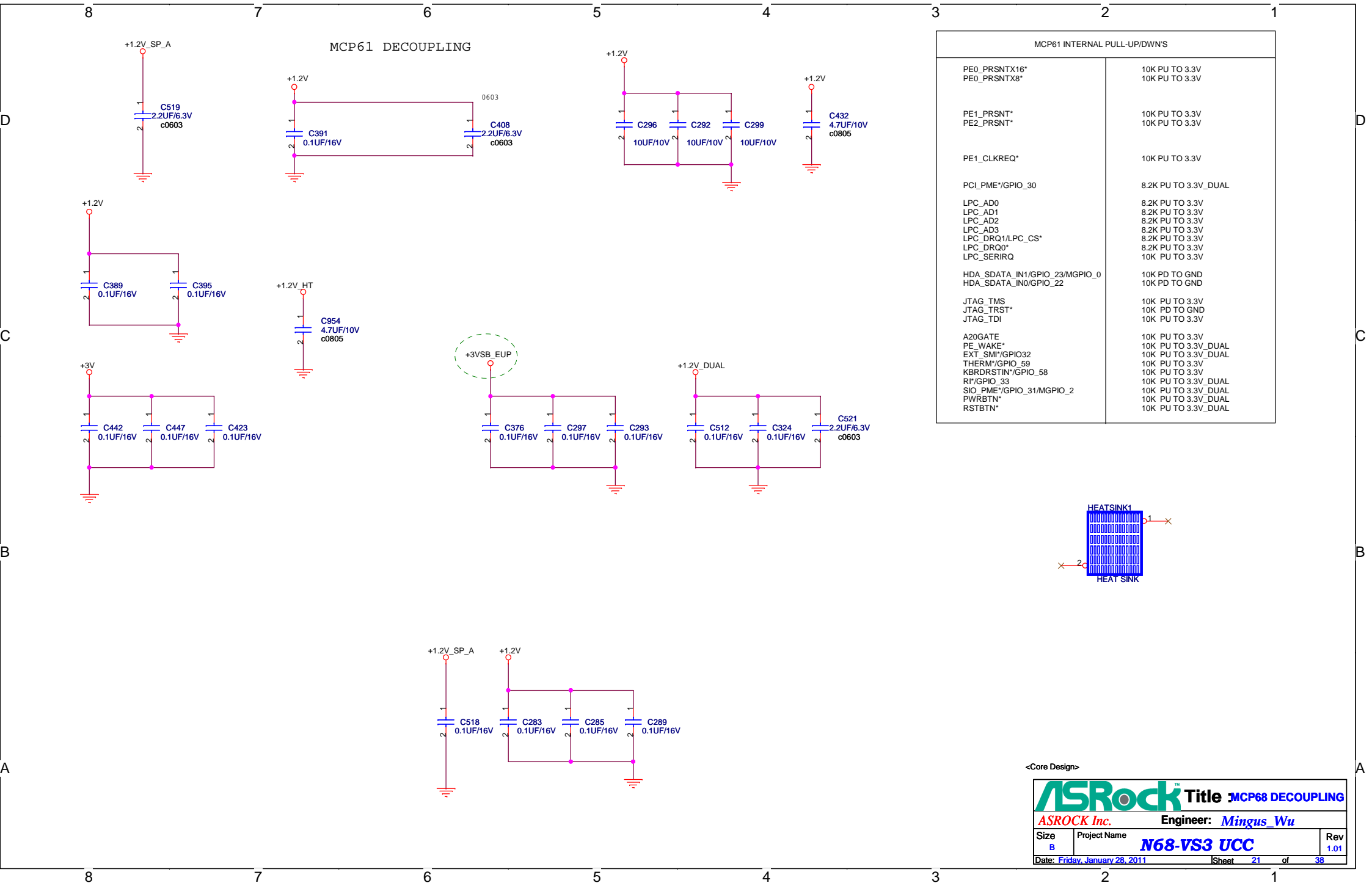


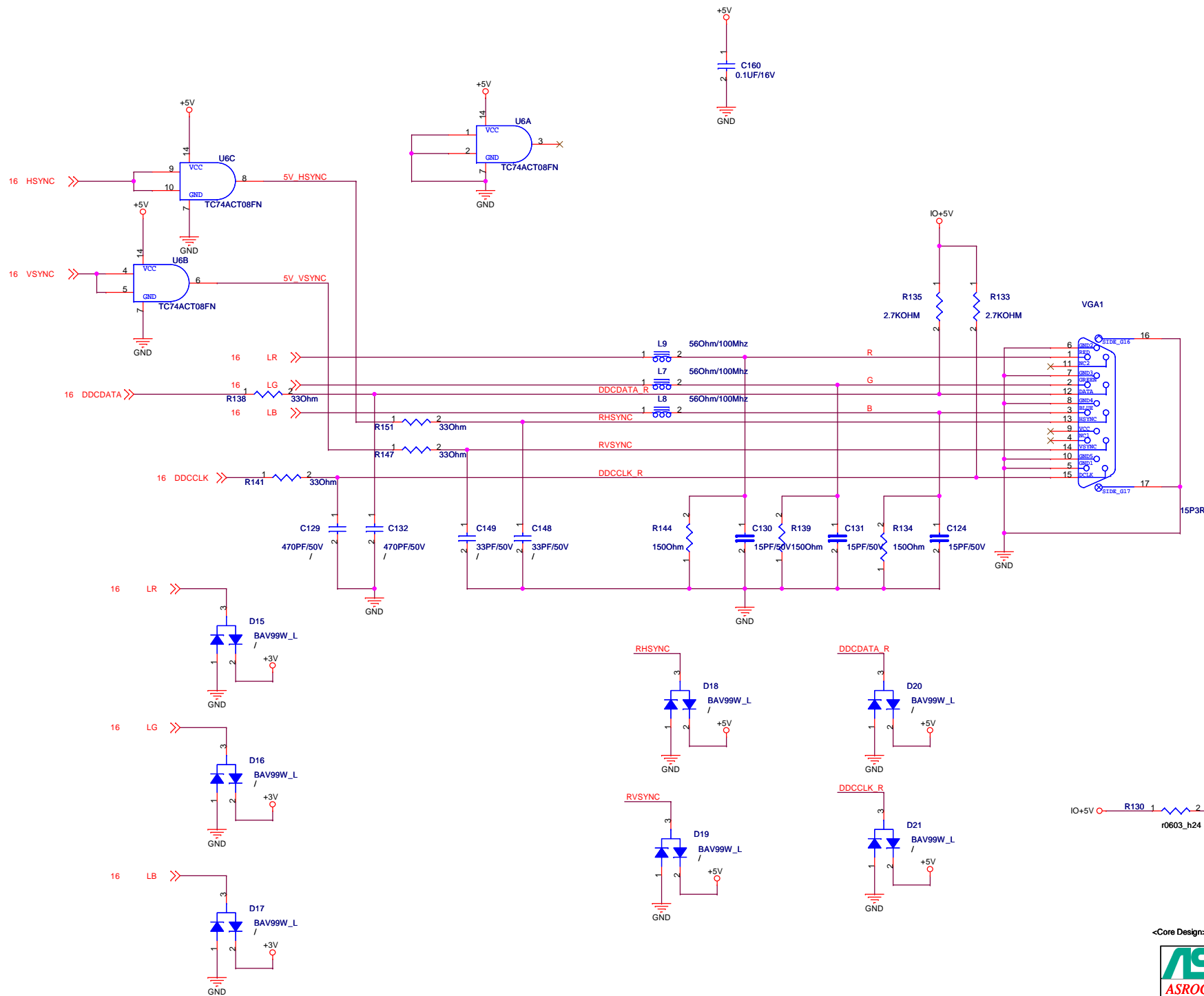
With AMT W/O AMT

+3V_CL +3V

S0-S5有電 S0有電

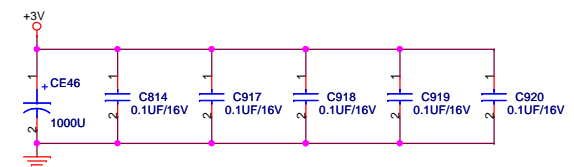
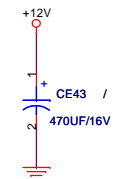
For one channel use.
Delete this block If you want to design one DIMM/channel.






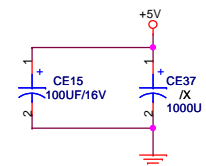
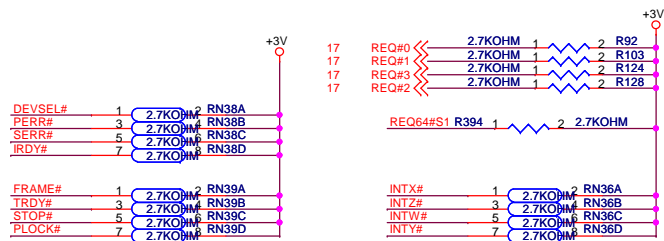
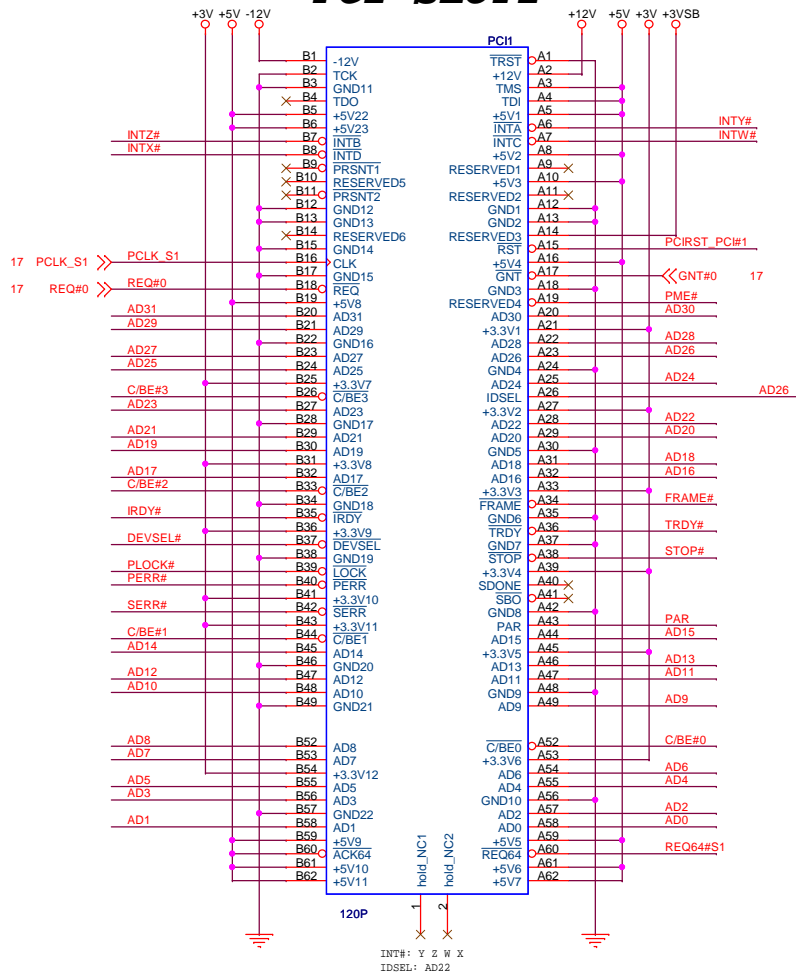
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ASRock Title : ON BORAD VGA	
ASRock Inc. Engineer: Mingus Wu	
Size A3	Project Name N68-VS3 UCC
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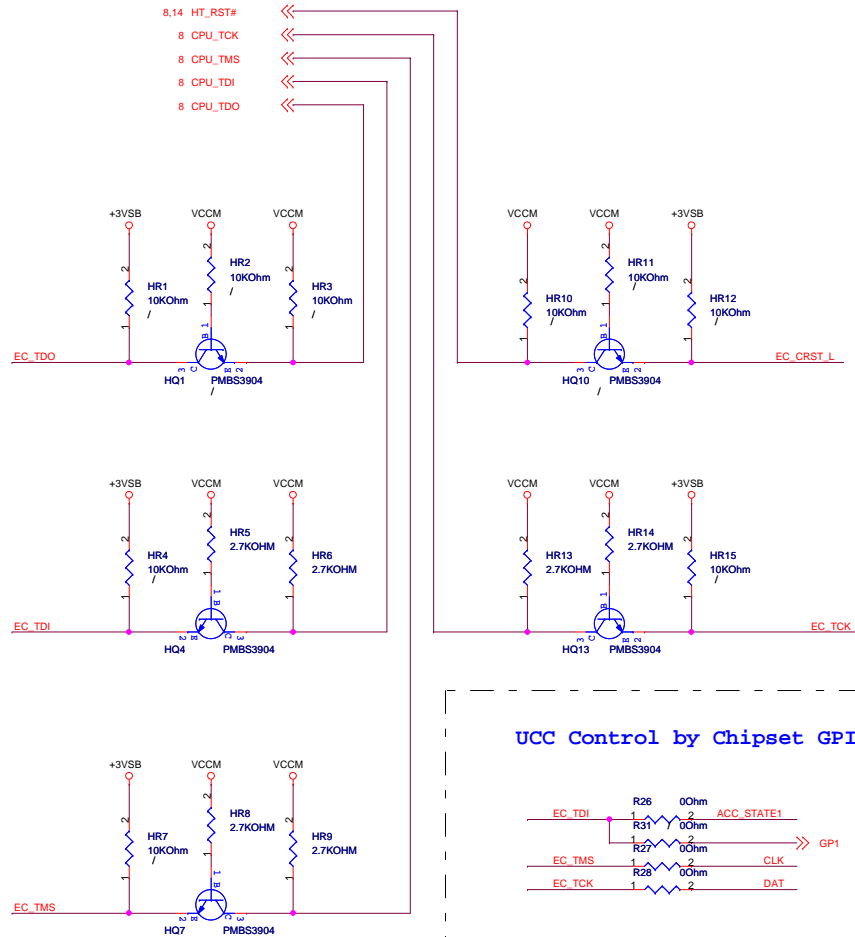
		Title : PCIE SLOT	
ASRock Inc.		Engineer: <u>Mingus Wu</u>	
Size A3	Project Name N68-VS3 UCC	Rev 1.01	
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PCI SLOT1

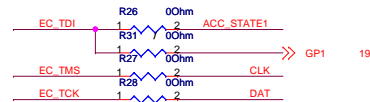


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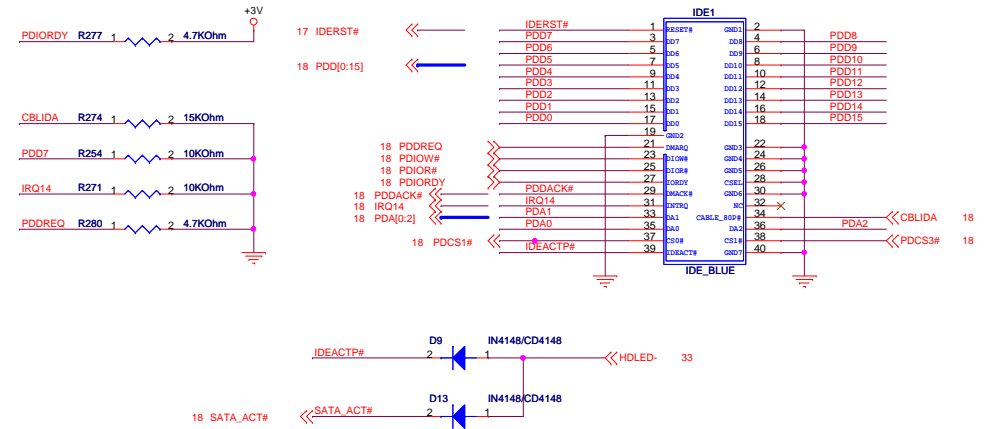
AMD OverDrive Level Translator



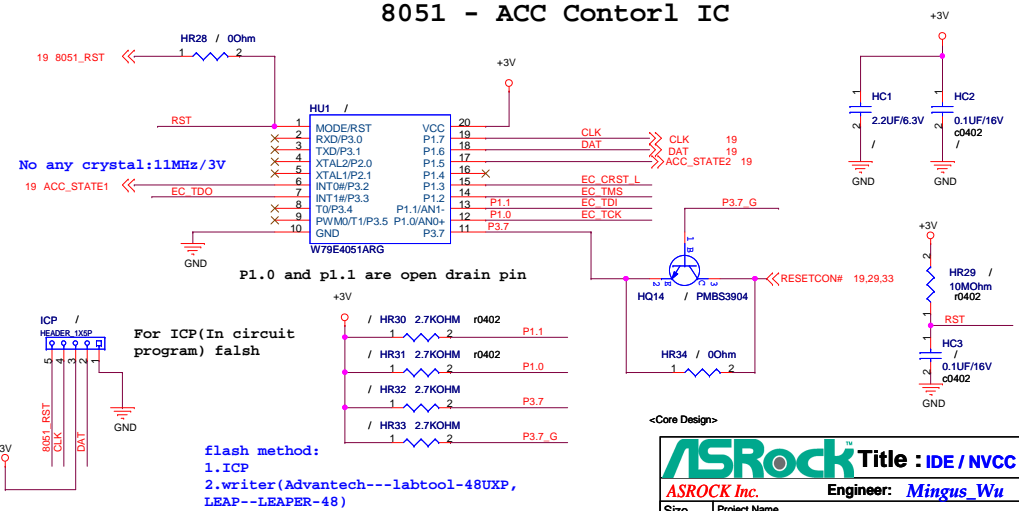
UCC Control by Chipset GPIO



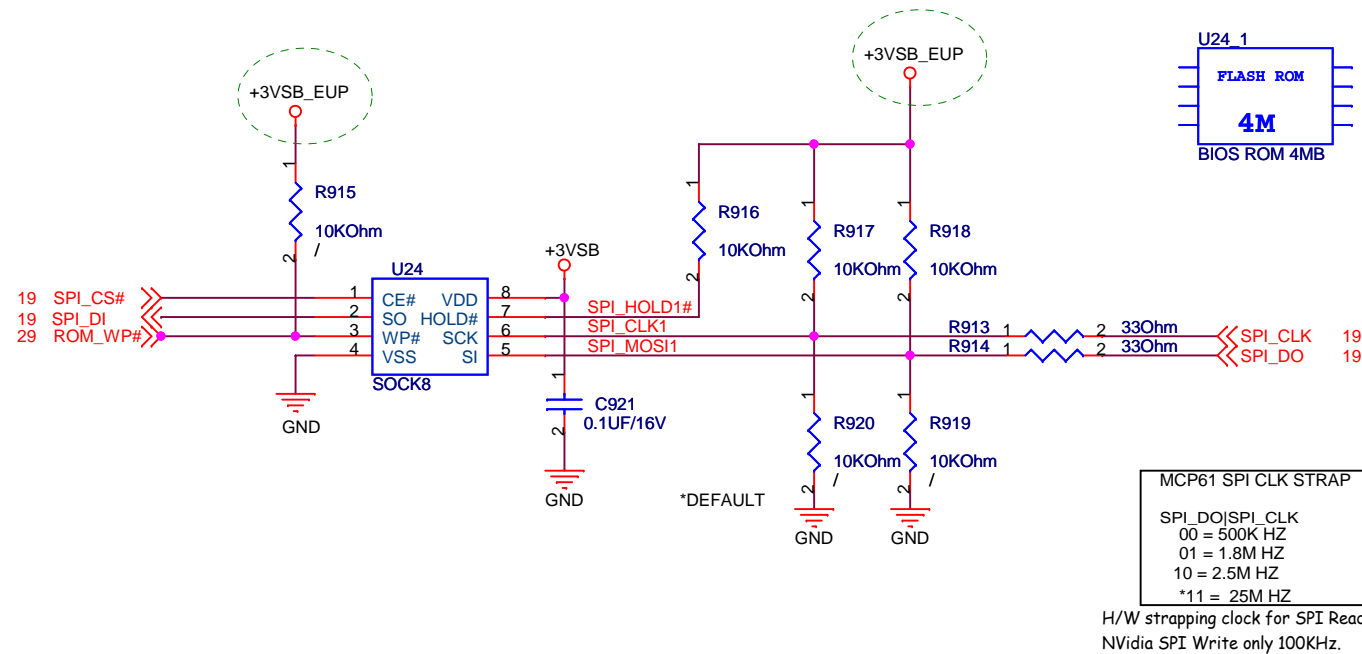
IDE1



8051 - ACC Contorl IC

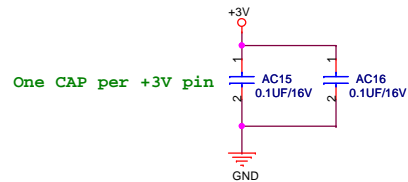
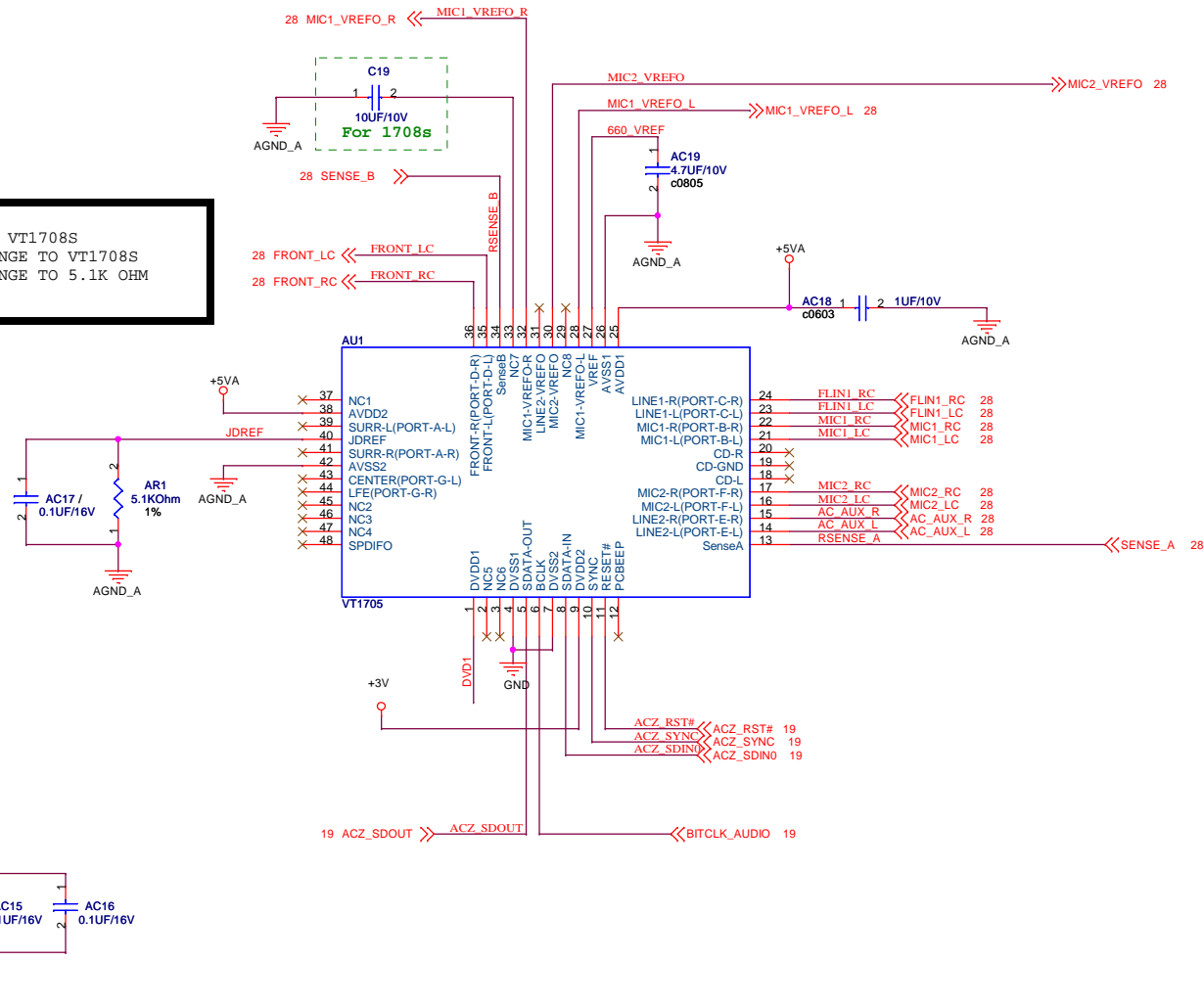


RSV for SPI

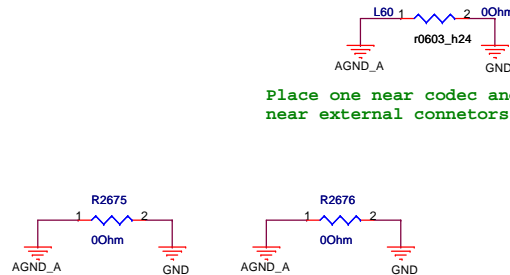


<Core Design>

CO-LAYOUT VT1708S
 AU1=> CHANGE TO VT1708S
 AR1=> CHANGE TO 5.1K OHM

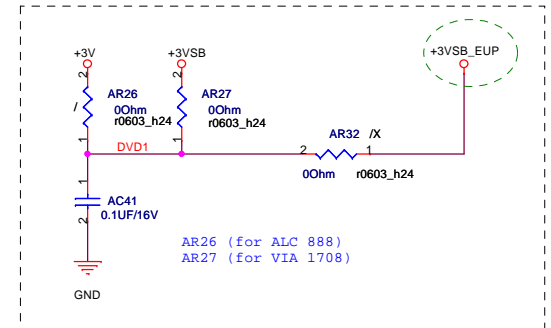
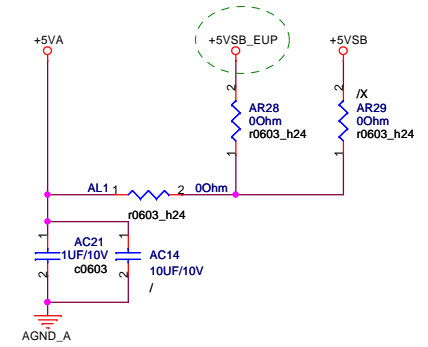


CD_R, D_GND and CD_L signal
 MUST away from other audio input
 signal for > 20mil to avoid
 crosstalk.



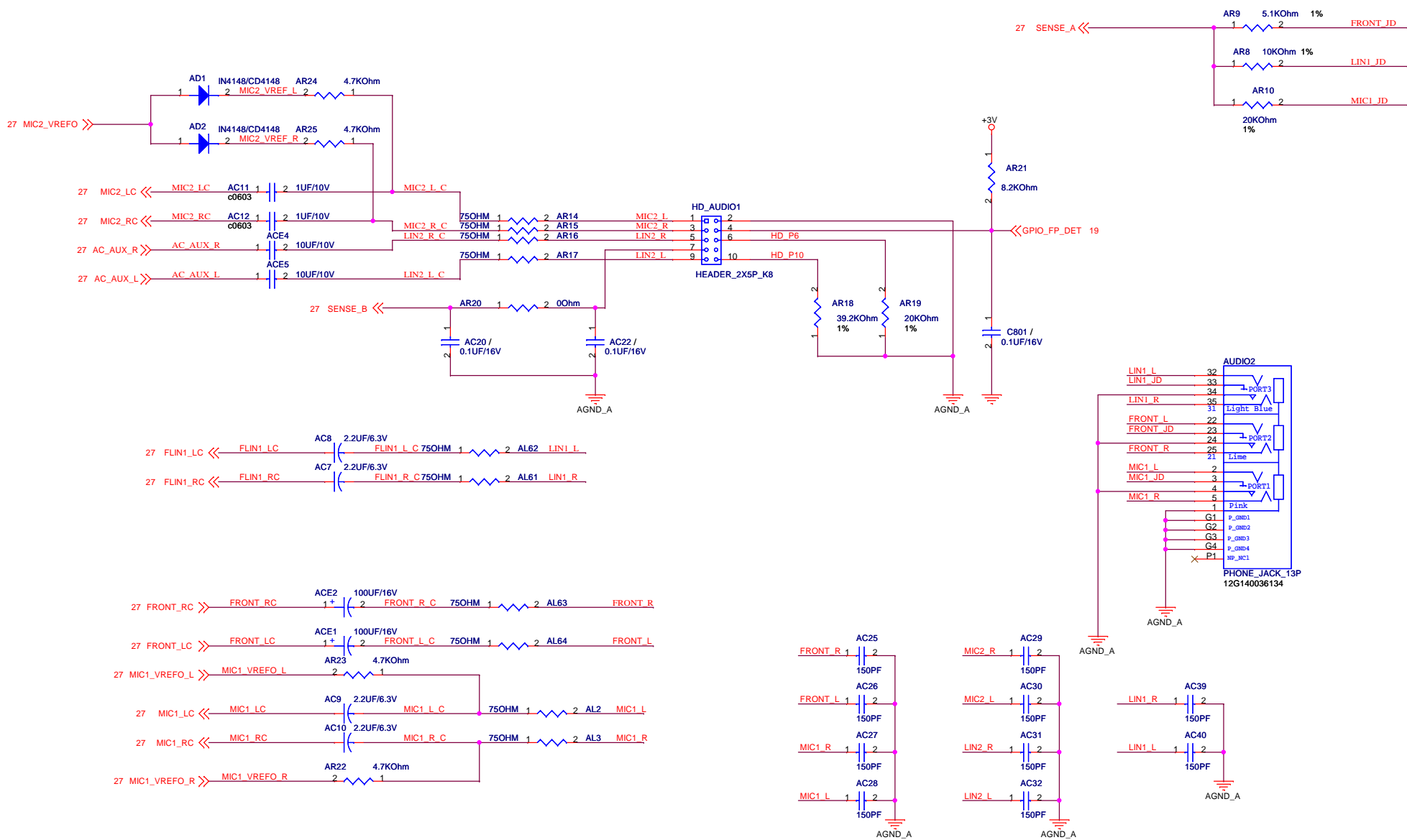
Place one near codec and another one
 near external connectors.

+5V Analog Power Switch

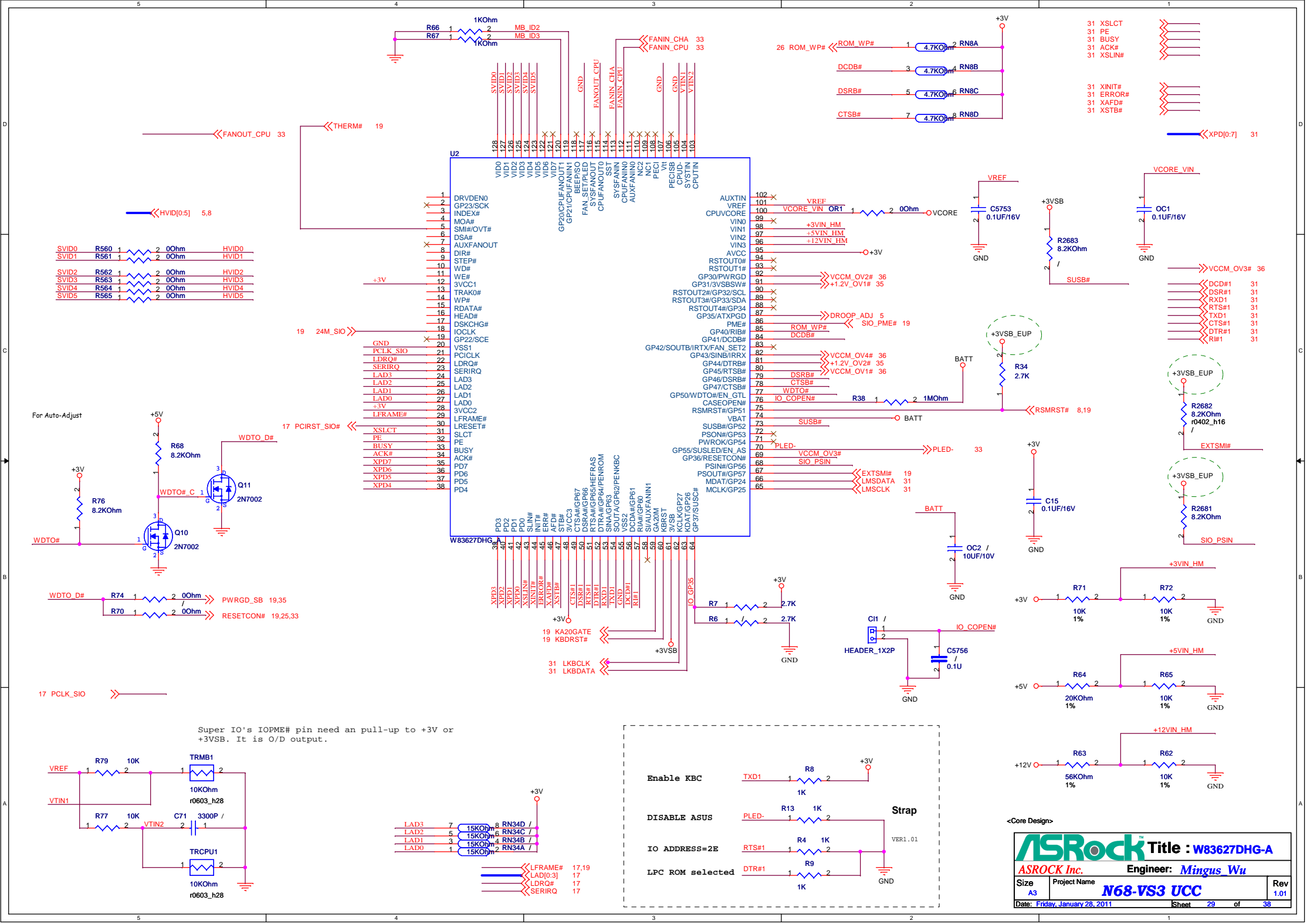


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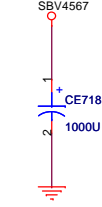
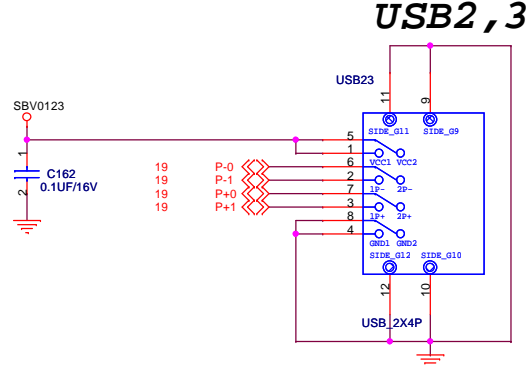
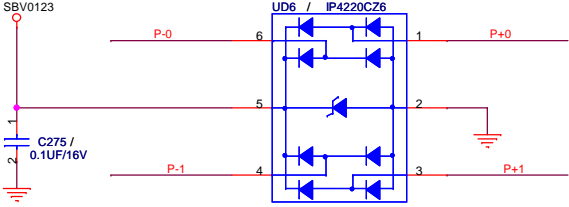
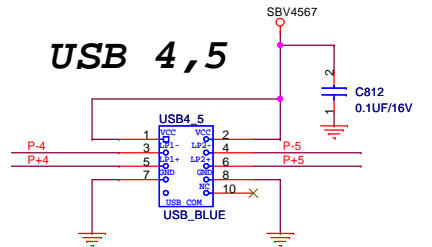
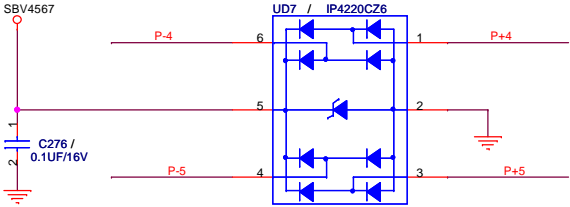
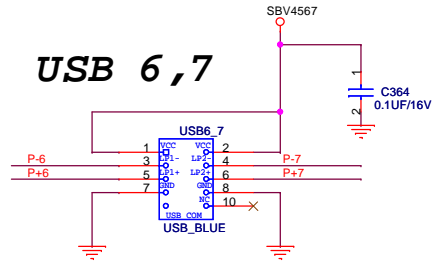
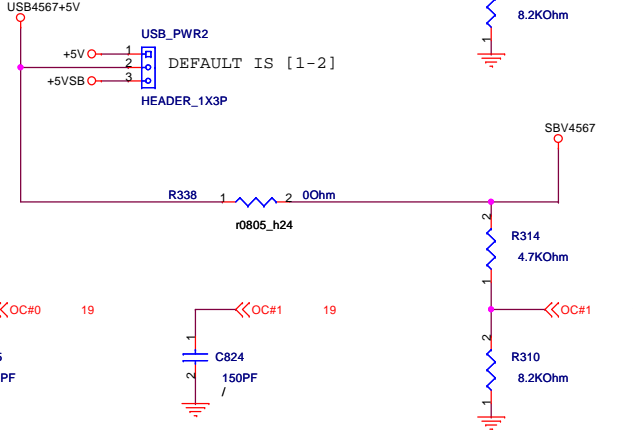
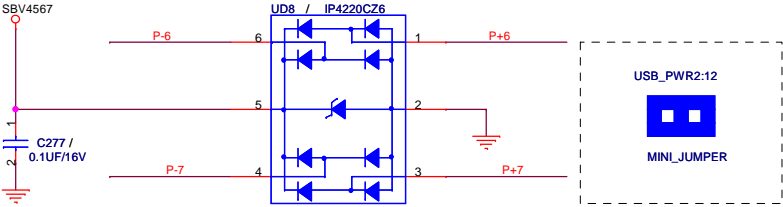
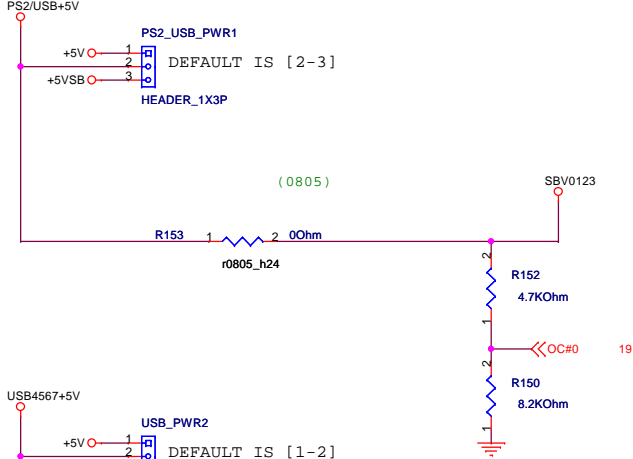
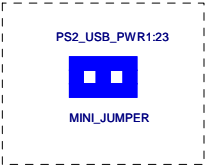
ASRock		Title : ALC888	
ASROCK Inc.		Engineer: Mingus Wu	
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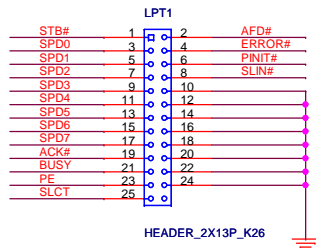
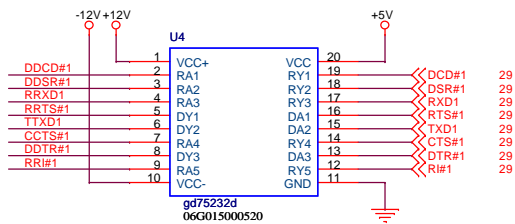


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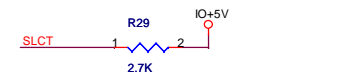
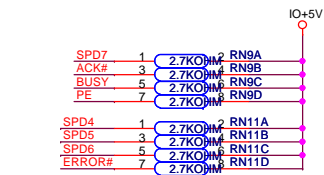
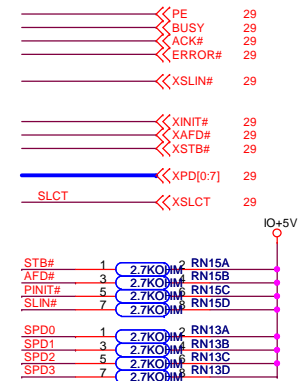
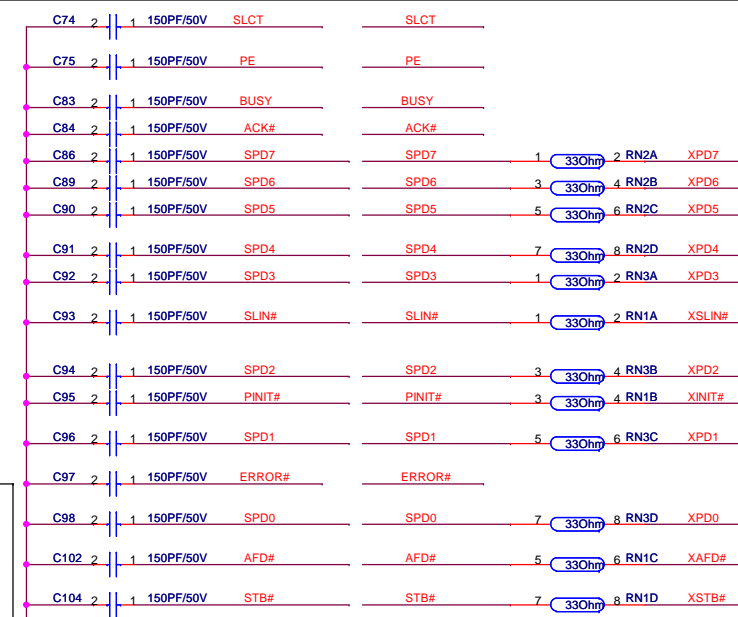
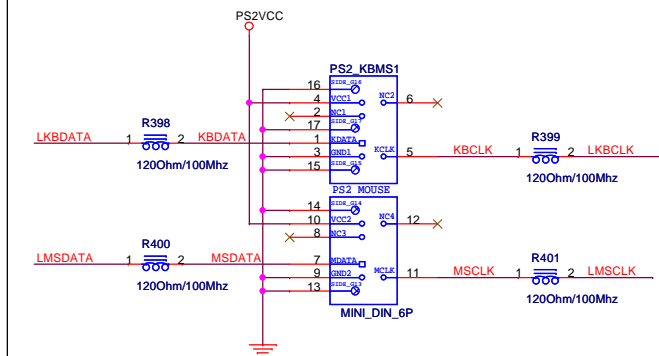
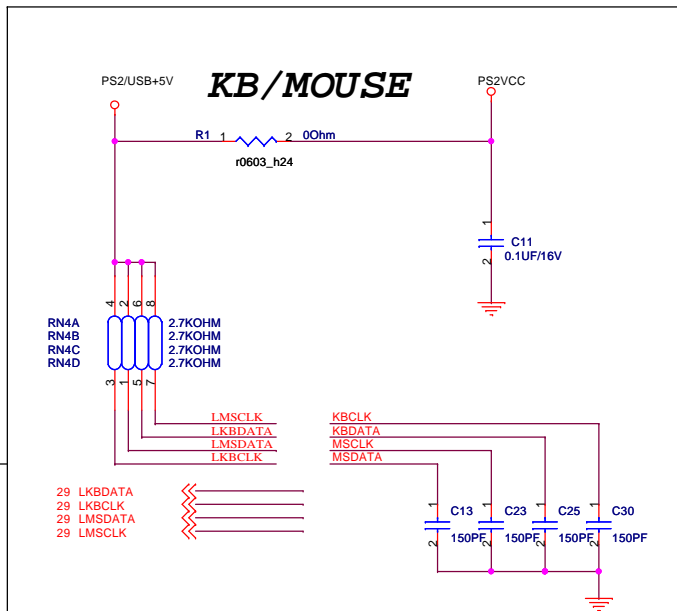
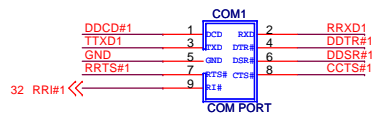
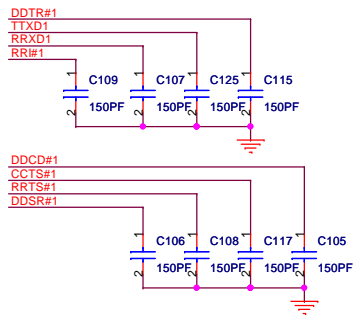


19 P+[4:7]
19 P-[4:7]





COM1

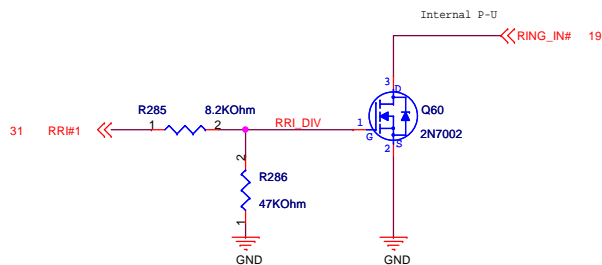
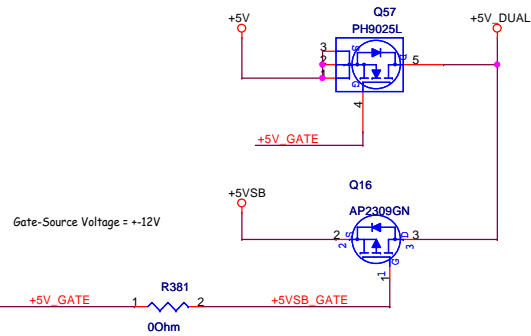
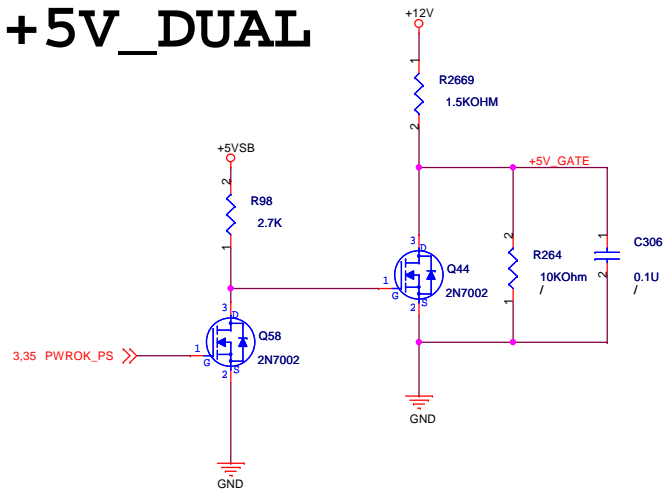


Parallel Port

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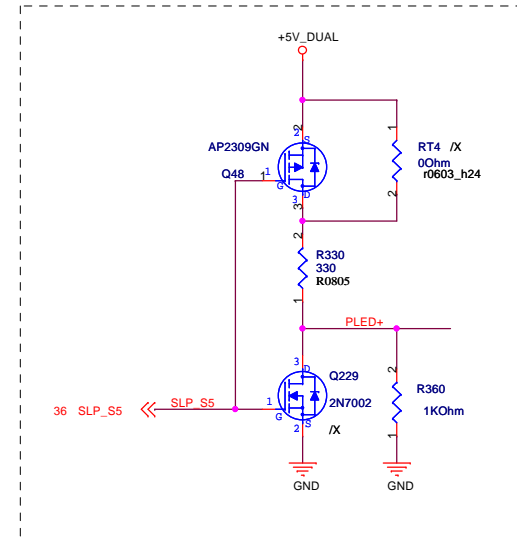
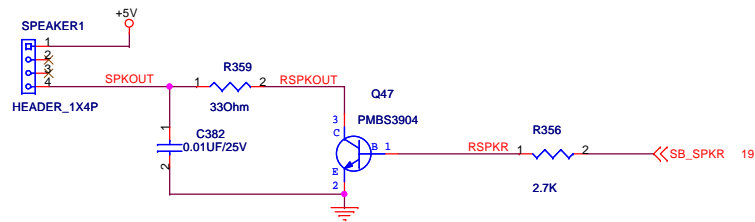
ASRock Title : IO CONNECTOR	
ASRock Inc. Engineer: Mingsu Wu	
Size A3	Project Name N68-VS3 UCC
Date: Friday, January 28, 2011	Sheet 31 of 38

+5V_DUAL



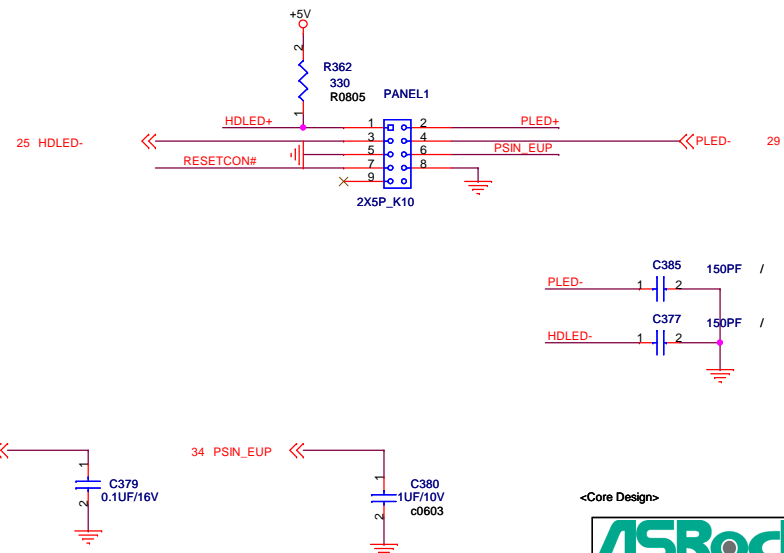
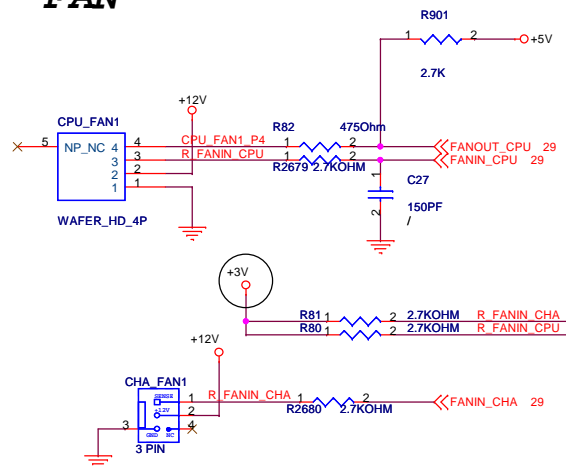
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ASRock		Title : POWER /S3	
ASRock Inc.		Engineer: Mingus_Wu	
Size A3	Project Name N68-VS3 UCC	Rev 1.01	
Date: Friday, January 28, 2011		Sheet 32	of 38



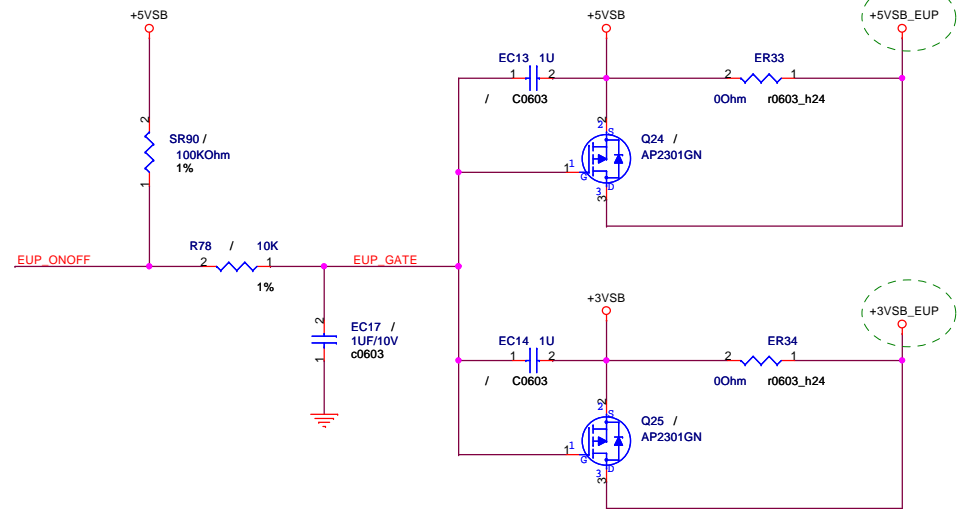
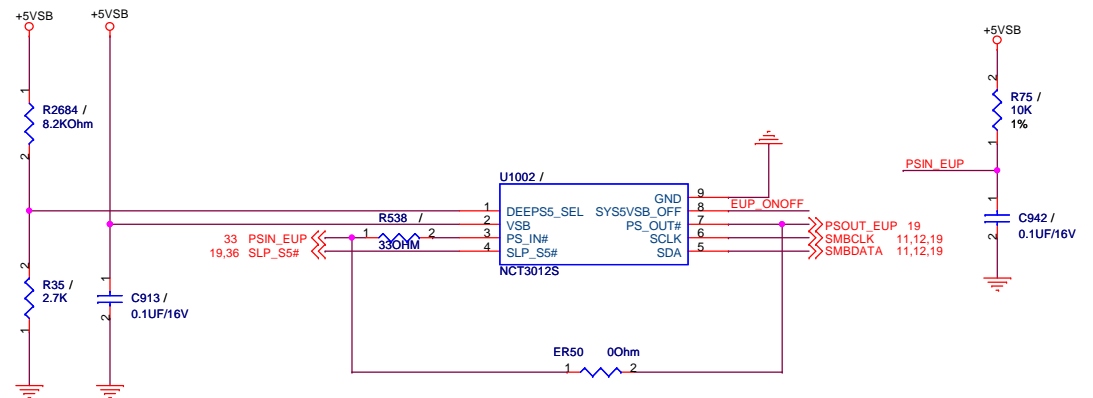
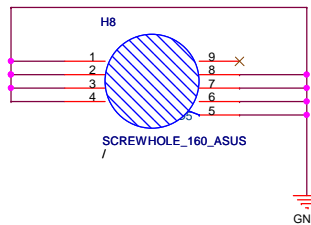
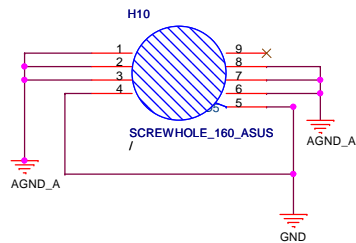
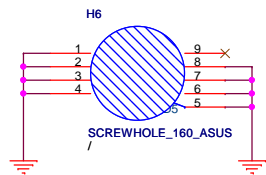
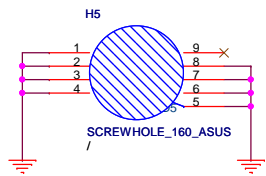
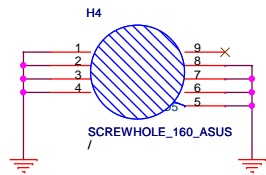
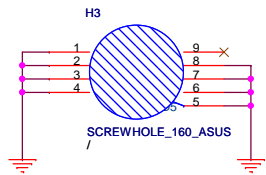
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FAN

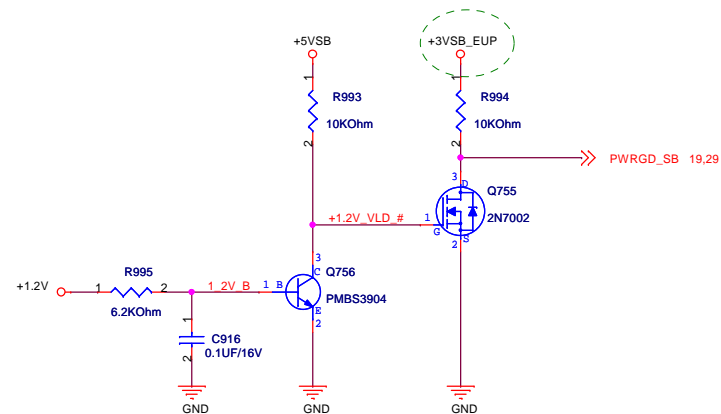
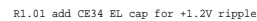
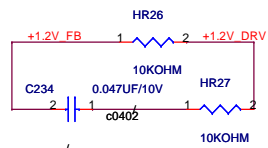


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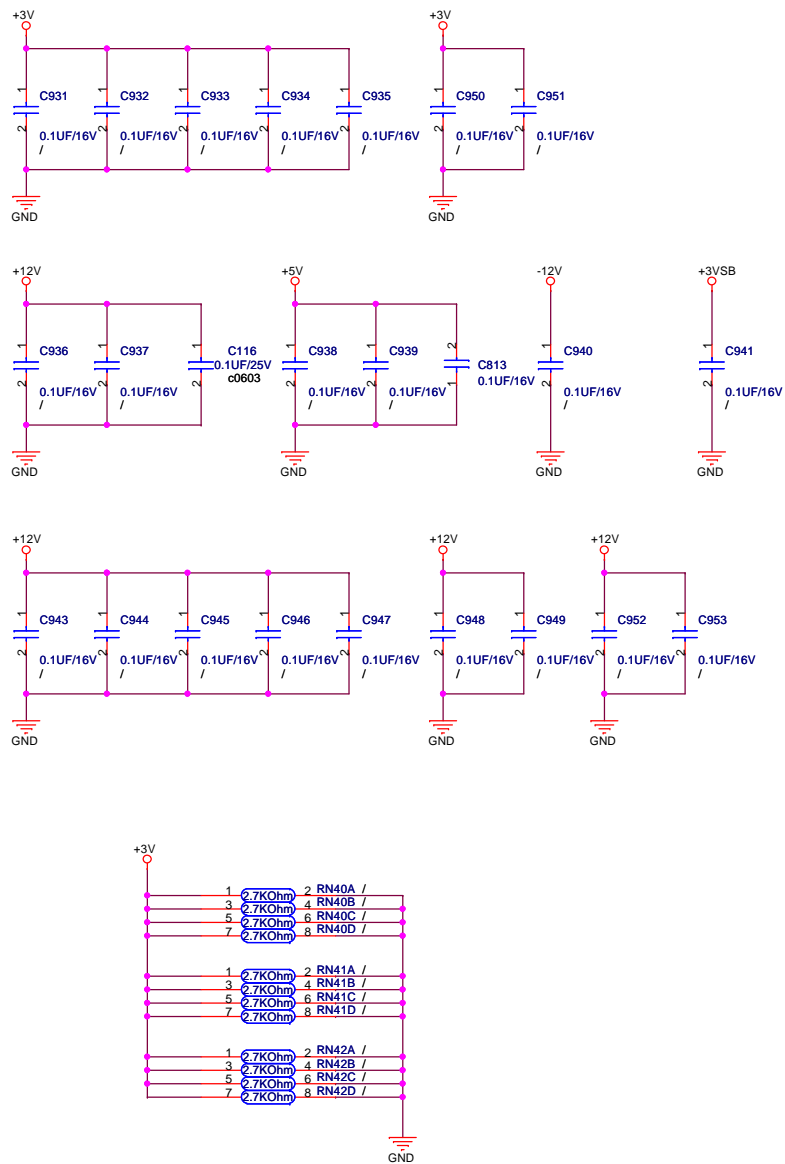
ASRock		Title : ROM / PANEL	
ASROCK Inc.		Engineer: <i>Mingus_Wu</i>	
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<Core Design>

ASRock ™		Title : ESD	
ASRock Inc.		Engineer: Mingus Wu	
Size	Project Name	Rev	
A3	N68-VS3 UCC	1.01	
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